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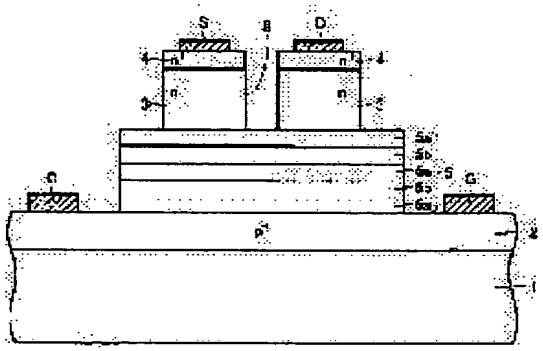
(54) JUNCTION FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a JFET (junction field effect transistor) which easily realizes normally off, while securing high conductance and where leakage current is small even at high temperatures, and to provide a method for manufacturing the JFET.
SOLUTION: The JFET is provided with a channel region 5 positioned at the path of an electric charge carrier between both of source and drain regions 4, and a p-conductive semiconductor layer 2 positioned in contact with the channel region 5, which is provided with an n-conductive undoped layer 5a and an conductive semiconductor layer 5b, having a concentration distribution projecting in a state of a pulse in the thickness direction in the undoped layer.



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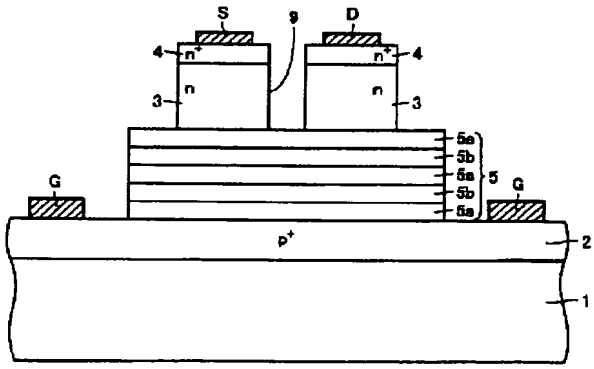
(54)【発明の名称】　接合型電界効果トランジスタおよびその製造方法

(57)【要約】
【課題】　高コンダクタンスを確保しつつノーマリーオフを容易に実現し、かつ高温でも漏洩電流の少ないＪＦＥＴおよびその製造方法を提供する。
【解決手段】　ソースおよびドレインの両領域４の間の電荷担体の経路に位置するチャネル領域５と、またチャネル領域５に接して位置するｐ導電型半導体層２とを備え、チャネル領域５が、ｎ導電型のアンドープ層５ａと、そのアンドープ層中に厚さ方向にパルス状に突出する濃度分布を有するｎ導電型半導体層５ｂとを備える。



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【特許請求の範囲】

【請求項１】　ソースおよびドレインの両領域の間の電荷担体の経路に設けられた第１導電型半導体のチャネル領域と、そのチャネル領域に接して位置する第２導電型半導体領域とを備える接合型電界効果トランジスタであって、

前記チャネル領域が、第１導電型のアンドープ層と、そのアンドープ層に上下面を挟まれるように位置し、厚さ方向の濃度分布がパルス状に突出する第１導電型半導体層とを備える、接合型電界効果トランジスタ。

【請求項２】　前記第２導電型半導体領域が、半導体基板およびその半導体基板上に成膜された薄膜のいずれかであり、前記チャネル領域がその第２導電型半導体領域の上に接して位置する、請求項１に記載の接合型電界効果トランジスタ。

【請求項３】　前記第２導電型半導体領域が、第１導電型半導体基板およびその半導体基板の上に接して成膜された第１導電型半導体膜のいずれかに、イオン注入法および不純物拡散法のいずれかにより第２導電型不純物を導入して形成されたものである、請求項１または２に記載の接合型電界効果トランジスタ。

【請求項４】　前記第２導電型半導体領域が、前記半導体基板の上に接して半導体膜をエピタキシャル成長させる間に第２導電型不純物を添加して形成した領域である、請求項１または２に記載の接合型電界効果トランジスタ。

【請求項５】　前記チャネル領域の厚さが、前記チャネル領域と前記第２導電型半導体領域との接合部の拡散電位で決まる空乏層の厚さよりも薄い、請求項１～３のいずれかに記載の接合型電界効果トランジスタ。

【請求項６】　前記半導体基板がＳｉＣ基板であり、前記各半導体を構成する結晶がＳｉＣである、請求項１～５のいずれかに記載の接合型電界効果トランジスタ。

【請求項７】　ソースとドレインとの両領域の間の電荷担体の経路にチャネル領域を有し、そのチャネル領域を通過する前記電荷担体の流れをゲート電圧によって制御する接合型電界効果トランジスタの製造方法であって、

前記ｎ導電型ＳｉＣ基板またはそのｎ導電型ＳｉＣ基板上に成膜されたｎ導電型ＳｉＣ薄膜に、イオン注入法によりｐ導電型不純物を導入するか、またはＳｉＣ薄膜のエピタキシャル成長中にｐ導電型不純物を添加するかしてｐ導電型ＳｉＣ層を形成する工程と、

前記ｐ導電型ＳｉＣ層の上に接してｎ導電型のＳｉＣアンドープ層と、そのＳｉＣアンドープ層にその上下面を挟まれるように位置し、厚さ方向の濃度分布がパルス状に突出するｎ導電型ＳｉＣ層とを含むチャネル層を形成する工程とを備える、接合型電界効果トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

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【発明の属する技術分野】本発明は、接合型電界効果トランジスタ(JFET:Junction Field Effect Transistor)およびその製造方法に関し、より具体的にはチャネル領域の不純物濃度分布を特別な分布とすることにより、高温漏れ電流の抑止や高コンダクタンスを確保することを図ったＪＦＥＴおよびその製造方法に関するものである。

【０００２】

【従来の技術】従来、ＪＦＥＴでは、図８に示すように、ソース電極Ｓに接続するｎ⁺導電型のソース領域１０４と、ドレイン電極Ｄに接続するｎ⁺導電型のドレイン領域１０４とは、それより不純物濃度の低いｎ導電型領域１０３で連続されている。とくに、ｎ導電型領域１０３の中央部は、溝１０９の底部に厚さを薄くされたチャネル領域１０７が設けられている。上記の構成は、ｐ⁺導電型半導体基板１０１の上に形成されたｐ⁺導電型層１０２の上に接して設けられている。また、半導体基板の裏面にはゲート電極Ｇが設けられている。

【０００３】上記の構成のＪＦＥＴを、たとえばスイッチング素子に用いる場合には、ゲート電極Ｇに負電位を印加して、ｐ⁺導電型薄膜１０２とチャネル領域１０９とのｐｎ接合に電圧を印加する。オフ状態を実現するためには、上記ｐｎ接合に逆バイアス電圧、すなわちｐ⁺導電型領域の電位をマイナス電位として、ｎ導電型領域の電位をプラス電位とする。この逆バイアス電圧の印加をｐ⁺ｎ接合に加えることによりｎ導電型領域１０７，１０３に空乏層を成長させ、チャネル厚さ全体を空乏層で遮断する。一方、オン状態を実現するためには、ゲート電圧をゼロまたは正電圧として、ソースドレイン間にチャネル領域を電荷担体が移動するように電圧を印加する。

【０００４】上述の説明では、ＪＦＥＴはノーマリーオンであると仮定して説明を行った。すなわち、ソース、ドレインおよびゲート電極に何も電圧を印加しなければ、チャネルに空乏層が張り出すことはなく、オン状態が実現している。しかし、上記のｐ⁺ｎ接合の拡散電位が大きく、チャネル厚さが十分薄い場合、拡散電位に起因する逆バイアス電圧により、チャネル領域の厚さ全体にわたって空乏層が形成される。この場合には、ソース、ドレインおよびゲート電極のいずれにも電圧を印加しなくても、オフ状態が実現する。このような、電圧を外部から印加しなくてもオフ状態が実現するＪＦＥＴをノーマリーオフのＪＦＥＴという。

【０００５】上記のＪＦＥＴは、半導体基板としてＳｉＣ基板を用いると、耐圧性に優れた高速スイッチング素子として用いることができる。

【０００６】

【発明が解決しようとする課題】しかし、オン状態で流せる電流はチャネル領域の厚さと幅と不純物濃度（キャリア濃度）で決まり、通常それほど大きな電流を流すこ

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とはできない。また、電流を大きくするためにチャネル領域の不純物濃度を高くすると、素子耐圧の低下をもたらす場合がある。また、チャネル領域の不純物濃度を高くすると、空乏層の張り出し厚さが小さくなりノーマリーオフを実現することができなくなる。逆に、ノーマリーオフを実現しようとすると、チャネル厚さを薄くし、かつチャネル領域の不純物濃度を低くしなければならない。この結果、コンダクタンスが低くなることは避けられない。

【０００７】一方、ＳｉＣなどの半導体の電子移動度を向上させるために、図９に示すように、チャネル領域１０７のアンドープ層１０７ａの中に、厚さ方向の濃度分布がデルタ関数的な面状の半導体層１０７ｂを離散的に持つ、いわゆるデルタドープの半導体層を持つＭＥＳＦＥＴ(Metal Semiconductor Field Effect Transistor)が提案されている（横川ら：第48回応用物理学関係連合講演会 講演予稿集30ａ-Ｅ-13、またJ. of Applied Physics, Vol89, p. 1794.)。デルタドープの名前は、パルス状またはスパイク状の分布を表わすデルタ関数に由来している。したがって、上記の濃度分布をデルタドープまたはパルスドープという場合もある。上記パルス状高濃度半導体層を含むチャネル領域１０７は、ＳｉＣ基板１０１の上に形成されたアンドープＳｉＣ層１０２の上に形成されている。

【０００８】上記ＭＥＳＦＥＴでは、ソース電極Ｓ、ドレイン電極Ｄはn^+ＳｉＣ層１０４とオーミック接続しているが、ゲート電極Ｇとアンドープ層１０７ｂとはショットキー接合されている。ゲート電極Ｇに印加される信号により、ショットキー障壁の空乏層厚さが変化して、ソース、ドレイン領域間を流れる電流が変化する。このようなデルタドープのチャネル領域を備えることにより、上記ＭＥＳＦＥＴは高い電子移動度をもつことができる。

【０００９】しかしながら、電流をショットキー電極によって制御するＭＥＳＦＥＴでは、ショットキー接合の障壁電位が低いために、温度上昇があると電流の漏れを生じてしまう。また、上述のようにノーマリーオフ型では、ショットキー電極と半導体との接合部に自然発生する拡散電位により空乏層を張り出し、チャネルを遮断してオフ状態とする。ショットキー接合の拡散電位は１Ｖ程度と低いために、空乏層の張り出し厚さは小さい。このため、この空乏層によってチャネルを遮断させるためには、チャネル厚さを相当薄くする必要がある。この結果、チャネルオン抵抗が大きく、コンダクタンスが小さくなってしまう。

【００１０】本発明は、高コンダクタンスを確保しつつノーマリーオフを容易に実現し、かつ高温でも漏洩電流の少ないＪＦＥＴおよびその製造方法を提供することを目的とする。

【００１１】

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【課題を解決するための手段】本発明のＪＦＥＴは、ソースおよびドレインの両領域の間の電荷担体の経路に設けられた第１導電型半導体のチャネル領域と、そのチャネル領域に接して位置する第２導電型半導体領域とを備えるＪＦＥＴである。このＪＦＥＴでは、チャネル領域が、第１導電型のアンドープ層と、そのアンドープ層に上下面を挟まれるように位置し、厚さ方向の濃度分布がパルス状に突出する第１導電型半導体層とを備える（請求項１）。

【００１２】（第２導電型チャネル領域/第１導電型半導体層）界面の拡散電位はショットキー接合の障壁電位差より数倍大きい。たとえば、半導体にＳｉＣを用いた場合、Ｔｉとのショットキー障壁電圧は１．１Ｖ～１．２Ｖである。これに比して、ｐｎ接合の拡散電位は約３Ｖに達する。このため、ショットキー接合を用いるＭＥＳＦＥＴよりも、高温での漏洩電流を各段に低くすることができる。

【００１３】また、厚さ方向パルス状の高濃度分布の第１導電型半導体層の形成により、電気抵抗を減らしより多くの電流を流すことができる。すなわち、高いコンダクタンスを確保することができる。さらに、チャネル領域の最上層は第１導電型アンドープ層なので、ソース、ドレイン領域を分ける溝をＲＩＥ(Reactive Ion Etching)法でエッチングする場合、寸法誤差があってもオン抵抗にほとんど影響しないようにできる。すなわち、高抵抗層と低抵抗層とが並列接続されている場合、高抵抗層に多少の変動があっても合成抵抗はほとんど影響は受けない。このため、ＲＩＥの加工精度の許容度を高め、製造歩留まりを向上させることができる。また、電子移動度もアンドープ層の濃度に依存するので、高い電子移動度を確保することができる。なお、上記の厚さ方向にパルス状に突出した濃度分布を持つ第１導電型半導体層は、上記アンドープ層にその上下面を挟まれるように接触されるかぎり、１層以上何層あってもよい。また、上記パルス状に高濃度の層の厚さは、アンドープ層の数分の一、たとえば、５分の１の厚さを有するようにする。

【００１４】上記本発明のＪＦＥＴでは、第２導電型半導体領域が、半導体基板およびその半導体基板上に成膜された薄膜のいずれかであり、チャネル領域が第２導電型半導体領域の上に接して位置することができる（請求項２）。

【００１５】この構成により、チャネル領域の下面から空乏層を張り出し、電荷担体の流れを容易に制御することができる。上記接合部に逆バイアス電圧を印加して空乏層を張り出させるゲート電極は、たとえば次の配置を有することができる。（ａ）チャネルと反対側の半導体基板の裏面にゲート電極を接続するバックゲート構造としてもよいし、また（ｂ）チャネルと同じ側のチャネルの両脇の一方または両方にゲート電極を接続する構造としてもよい。

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【００１６】上記本発明のＪＦＥＴでは、第２導電型半導体領域を、第１導電型半導体基板およびその半導体基板の上に接して成膜された第１導電型半導体膜のいずれかに、イオン注入法および不純物拡散法のいずれかにより第２導電型不純物を導入して形成されたものとできる（請求項３）。

【００１７】ｐ導電型ＳｉＣ膜は、ボロンをドーパントとしてエピタキシャル成長法で形成するとき、マイクロパイプなどを多く含み、結晶性が非常に悪いものしかできない場合がある。また、アルミニウムをドーパントとする場合、アルミニウムが成膜装置の内壁に堆積するため、定期的にクリーニングする必要があり、製造能率が低下する。上記の製造方法により、半導体をＳｉＣとし、第２導電型をｐ導電型とした場合でも、結晶性の良好なｐ導電型ＳｉＣ層をチャネル領域の下に、間違いなく高い生産性の下で形成することができる。この結果、高温での漏洩電流を抑制することができる。

【００１８】上記本発明のＪＦＥＴでは、第２導電型半導体領域を、半導体基板の上に接して半導体膜をエピタキシャル成長させる間に第２導電型不純物を添加して形成した領域とすることができる（請求項４）。

【００１９】この構成により、たとえばｐ導電型ＳｉＣ膜を重大な欠陥なくエピタキシャル成長させる条件を見出すことができた場合などに、このｐ導電型ＳｉＣ膜を用いてＪＦＥＴを形成することができる。

【００２０】上記本発明のＪＦＥＴでは、チャネル領域の厚さが、チャネル領域と第２導電型半導体領域との接合部の拡散電位で決まる空乏層の厚さよりも薄くすることができる（請求項５）。

【００２１】この構成により、(1) アンドープ層の第１導電型不純物濃度と、(2) デルタドープ層の第１導電型不純物濃度と、(3) 第２導電型半導体層の第２導電型不純物濃度とを調整して接合部の拡散電位を知り、接合部においてチャネル側に張り出す空乏層の厚さを知ることができる。この空乏層の厚さよりも (4) チャネル領域の厚さを薄くすることにより、ノーマリーオフのＪＦＥＴを製造することができる。ノーマリーオフのＪＦＥＴは、電気回路系に故障を生じ配電されない場合にオフ状態とできるので、回路を複雑にすることなく回転機等の制御に用いることができる。

【００２２】上記本発明のＪＦＥＴでは、半導体基板をＳｉＣ基板とし、各半導体を構成する結晶をＳｉＣとできる（請求項６）。

【００２３】ＳｉＣは耐圧性能に優れ、電荷担体の移動度も高いので、大電力の制御や大電力の高速スイッチング素子に用いることができる。

【００２４】本発明のＪＦＥＴの製造方法では、ソースとドレインとの両領域の間の電荷担体の経路にチャネル領域を有し、そのチャネル領域を通過する電荷担体の流れをゲート電圧によって制御する接合型電界効果トランジスタの製造方法である。この製造方法は、ｎ導電型ＳｉＣ基板またはそのｎ導電型ＳｉＣ基板上に成膜されたｎ導電型ＳｉＣ薄膜に、イオン注入法および拡散法のいずれかによりｐ導電型不純物を導入するか、またはＳｉＣ薄膜のエピタキシャル成長中にｐ導電型不純物を添加するかしてｐ導電型ＳｉＣ層を形成する工程と、ｐ導電型ＳｉＣ層の上に接してｎ導電型のＳｉＣアンドープ層と、そのＳｉＣアンドープ層にその上下面を挟まれるように位置し、厚さ方向の濃度分布がパルス状に突出するｎ導電型ＳｉＣ層とを含むチャネル層を形成する工程とを備える（請求項７）。

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【００２５】この製造方法により、結晶性に優れた厚さ方向パルス状の高濃度分布の第１導電型半導体層の形成により、高いコンダクタンスを確保したＪＦＥＴを容易に形成することができる。さらに、チャネル領域の最上層は第１導電型アンドープ層なので、たとえばソース、ドレイン領域を分ける溝を形成する場合、ＲＩＥ(Reactive Ion Etching)法でエッチングするとき、寸法誤差があってもオン抵抗にほとんど影響しないようにできる。すなわち、高抵抗層と低抵抗層とが並列接続されている場合、高抵抗層に多少の変動があっても合成抵抗はほとんど影響は受けない。このため、ＲＩＥの加工精度の許容度を高め、製造歩留まりを向上させることができる。

【００２６】

【発明の実施の形態】次に図面を用いて本発明の実施の形態について説明する。

（実施の形態１）図１は、本発明の実施の形態１におけるＪＦＥＴを示す断面図である。ＳｉＣ基板１の上にp^+導電型ＳｉＣ膜２が形成されている。そのp^+導電型ＳｉＣ膜２の上に、アンドープ層である厚さ５０ｎｍのｎ導電型ＳｉＣ膜５ａと、厚さ１０ｎｍの急峻な濃度分布を有するn^+導電型のパルス状層５ｂとが、交互に積層されている。図２に、チャネル領域の厚さ方向のｎ導電型不純物濃度の分布を示す。この積層領域がチャネル領域５を構成する。n^+導電型のパルス状層５ｂは、デルタ層、パルス状層、またはスパイク状層と呼ぶこともある。このデルタ層のｎ型不純物濃度のピーク値は、$1\times10^{18}\,cm^{-3}$である。アンドープ層のｎ導電型不純物濃度は、このピーク値の濃度より数オーダー低い。チャネル層５の最も上の部分およびp^+導電型ＳｉＣ膜２と接する最も下の部分は、アンドープ層によって形成されている。

【００２７】チャネル層５の上に、分かれて位置するソース電極Ｓ、ドレイン電極Ｄに接続するn^+導電型領域４、およびその下に位置してチャネル領域と接するｎ導電型半導体領域３が配置されている。

【００２８】図１の構造の場合、ＳｉＣ基板の上に形成されたp^+導電型ＳｉＣ膜の上にゲート電極Ｇが配置されている。

【００２９】上記の構造のＪＦＥＴでは、p^+導電型Ｓ

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ｉＣ膜２とチャネル領域の最下層のアンドープ層５ａとの接合部に、約３Ｖの拡散電位を生じる。この拡散電位は、上記接合部に逆バイアス電圧として作用するので、ＭＥＳＦＥＴのショットキー障壁電位による漏洩電流防止に比べて、より高温まで確実に漏洩電流を抑制することができる。さらに、高濃度不純物のデルタ層の形成により、電気抵抗を減らし、より多くの電流を流すことができる。すなわち、高いコンダクタンスを確保することができる。また、電子の移動度もアンドープ層の濃度に依存するので、高い電子移動度を確保することができる。

【００３０】上記図１の構造は、次の製造方法により製造することができる。

(1)まず、ｎ導電型ＳｉＣ基板またはＳｉＣ基板上に形成したｎ導電型ＳｉＣ膜に、ｐ導電型不純物をイオン注入法により導入するか。またはｐ導電型不純物を添加しながらＳｉＣ膜をエピタキシャル成長して、ｐ導電型ＳｉＣ層を形成する。この結果、結晶性の良好なｐ導電型ＳｉＣ膜を得ることができる。

(2)次いで、ｎ導電型アンドープＳｉＣ層とパルス状ｎ導電型ＳｉＣ層とを交互に形成する。チャネル領域の最下層と最上層とはアンドープ層とする。パルス状のｎ導電型不純物濃度のピーク値は、$1\times10^{18}cm^{-3}$とする。

(3)この後、ソース、ドレイン領域となるｎ導電型ＳｉＣ層を成膜する。このｎ導電型ＳｉＣ膜をＲＩＥ(Reactive Ion Etching)などのドライエッチングによりエッチングすることにより、チャネル領域５をパターニングする。

(4)次いで、通常の方法により、チャネル領域の上にソース、ドレインを分離して形成する。また、ゲート電極Ｇをｐ⁺導電型ＳｉＣ膜２の上に形成する。

【００３１】上記の製造方法により、良好な結晶性のｐ導電型ＳｉＣ膜を得ることができる。

【００３２】図３は、上記本発明の実施の形態１のＪＦＥＴの変形例を示す図である。このＪＦＥＴでは、ＳｉＣ基板にｐ導電型不純物を導入し、その上に直接、チャネル領域５を配置している。

【００３３】また、図４は、上記本発明の実施の形態１のＪＦＥＴの別の変形例を示す図である。このＪＦＥＴでは、ＳｉＣ基板には、ｐ導電型不純物を導入し、ｐ導電型ＳｉＣ基板とする。さらに、ゲート電極は、ｎ⁺導電型ＳｉＣ基板の裏面側にオーミック接続されたバックゲート構造とされている。このようなバックゲート構造を用いることにより、ＪＦＥＴの２次元寸法を減らし、小型化することが可能となる。

（実施の形態２）図５は、本発明の実施の形態２におけるＪＦＥＴを示す断面図である。このＪＦＥＴは、ノーマリーオフ型のＪＦＥＴであり、このため、パルス状濃度の層は１層のみとしている。１層のパルス状高濃度ｎ

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型半導体層５ｂと、それを上下から挟むｎ導電型アンドープ層５ａとからなるチャネル領域５の厚さは、ノーマリーオフが実現される厚さとされている。すなわち、チャネル領域とｐ⁺導電型ＳｉＣ層との接合部に発生する拡散電位のために、この接合部に空乏層が発生し、所定厚さだけチャネル領域に伸びる。この所定厚さの空乏層によって、上記チャネル領域が遮断されるようにすれば、ノーマリーオフのＪＦＥＴが実現される。

【００３４】上記の拡散電位は、ＳｉＣの場合、約３Ｖと比較的高い。ＭＥＳＦＥＴにおけるショットキー電位が１．１Ｖ～１．２Ｖなので、それより数倍高い逆バイアス電圧を得ることができる。上記の空乏層の厚さは、逆バイアス電圧に比例するので、ＪＦＥＴの拡散電位約３ＶのほうがＭＥＳＦＥＴのショットキー電圧１．１からよりも相当高いので、チャネル厚さを従来よりも厚くしてＪＦＥＴを形成することができる。このため、ノーマリーオフのＭＥＳＦＥＴよりも、ノーマリオフのＪＦＥＴのほうが、高いコンダクタンスを確保することができる。

【００３５】図５のノーマリーオフのＪＦＥＴも、基本的に図１のＪＦＥＴと同様な製造方法により製造することが可能である、図６は、上記本発明の実施の形態２におけるノーマリーオフのＪＦＥＴの変形例を示す図である。このＪＦＥＴでは、ＳｉＣ基板にｐ導電型不純物を導入したｐ導電型ＳｉＣ基板を用いている。このため、ＳｉＣ基板の上にｐ⁺導電型ＳｉＣ膜を形成する必要がないので、１工程省略することができる。

【００３６】また、図７は、上記本発明の実施の形態２におけるノーマリーオフのＪＦＥＴの別の変形例を示す図である。このＪＦＥＴでは、ＳｉＣ基板にｐ導電型不純物を導入し、ｐ導電型ＳｉＣ基板を用いている。さらに、ゲート電極は、ｎ⁺導電型ＳｉＣ基板の裏面側にオーミック接続されたバックゲート構造とされている。このようなバックゲート構造を用いることにより、ＪＦＥＴの２次元寸法を減らし、小型化することが可能となる。

【００３７】上記において、本発明の実施の形態について説明を行ったが、上記に開示された本発明の実施の形態は、あくまで例示であって、本発明の範囲はこれら発明の実施の形態に限定されない。本発明の範囲は、特許請求の範囲の記載によって示され、さらに特許請求の範囲の記載と均等の意味および範囲内でのすべての変更を含むものである。

【００３８】

【発明の効果】本発明のＪＦＥＴおよびその製造方法を用いることにより、高コンダクタンスを確保しつつノーマリーオフを容易に実現し、かつ高温でも漏洩電流の少ないＪＦＥＴを提供することができる。

【図面の簡単な説明】

【図１】　本発明の実施の形態１におけるＪＦＥＴの断

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面図である。

【図２】　チャネル領域の厚さ方向のｎ導電型不純物濃度の分布を示す図である。

【図３】　本発明の実施の形態１におけるＪＦＥＴの変形例の断面図である。

【図４】　本発明の実施の形態１におけるＪＦＥＴのさらに別の変形例の断面図である。

【図５】　本発明の実施の形態２におけるＪＦＥＴの断面図である。

【図６】　本発明の実施の形態２におけるＪＦＥＴの変形例の断面図である。

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【図７】　本発明の実施の形態２におけるＪＦＥＴのさらに別の変形例の断面図である。

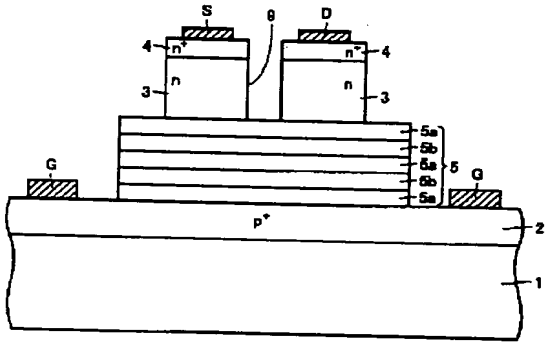
【図８】　従来のＪＦＥＴを示す断面図である。

【図９】　従来のＭＥＳＦＥＴを示す断面図である。

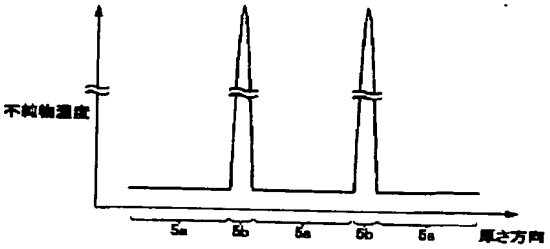
【符号の説明】

１　ＳｉＣ基板、２　ｐ+導電型ＳｉＣ膜、３　ｎ導電型ＳｉＣ層、４　ｎ導電型ＳｉＣ層、５　チャネル層、５ａ　ｎ導電型アンドープ層、５ｂ　パルス状高濃度ｎ型ＳｉＣ層、Ｓ　ソース電極、Ｄ　ドレイン電極、Ｇ　ゲート電極。

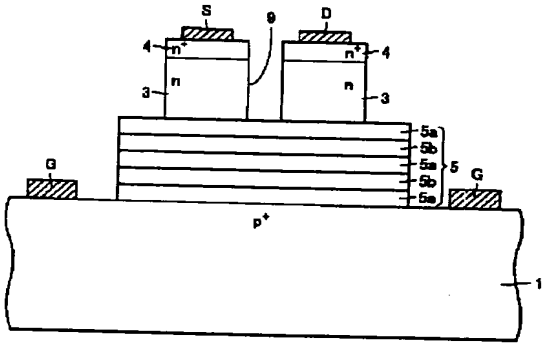
【図１】



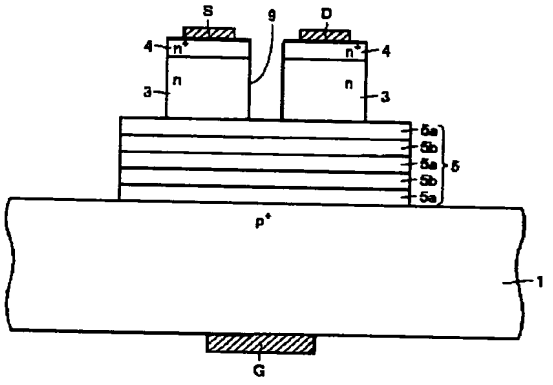
【図２】



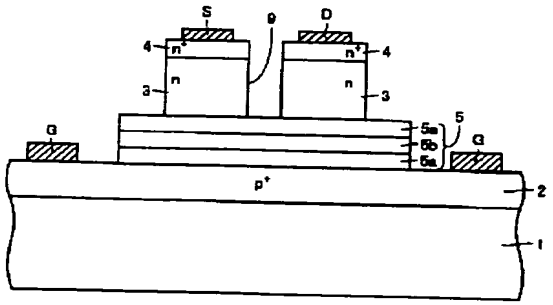
【図３】



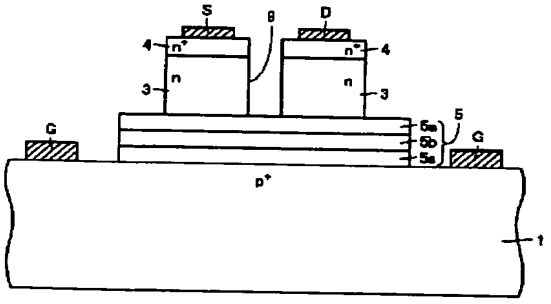
【図４】



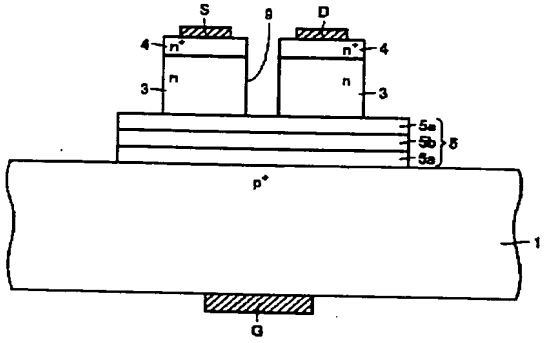
【図５】



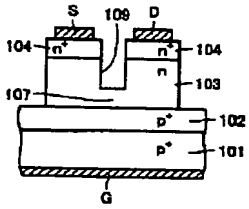
【図６】



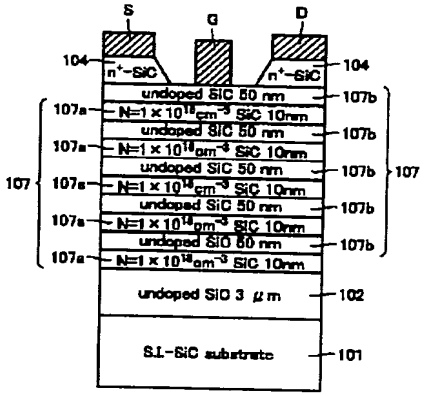
【図７】



【図８】



【図９】



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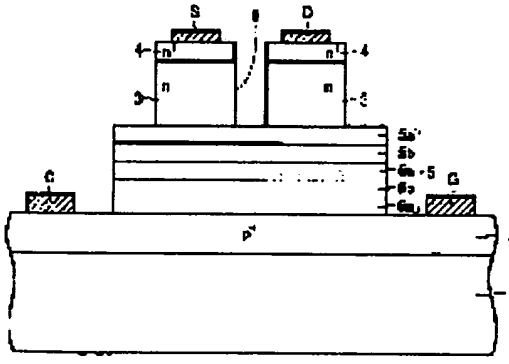
(54) JUNCTION FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING THE SAME



(57)Abstract:
PROBLEM TO BE SOLVED: To provide a JFET (junction field effect transistor) which easily realizes normally off, while securing high conductance and where leakage current is small even at high temperatures, and to provide a method for manufacturing the JFET.
SOLUTION: The JFET is provided with a channel region 5 positioned at the path of an electric charge carrier between both of source and drain regions 4, and a p-conductive semiconductor layer 2 positioned in contact with the channel region 5, which is provided with an n-conductive undoped layer 5a and an conductive semiconductor layer 5b, having a concentration distribution projecting in a state of a pulse in the thickness direction in the undoped layer.

LEGAL STATUS

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[Date of extinction of right]	

CLAIMS

[Claim(s)]
[Claim 1] The junction field effect transistor which it is a junction field effect transistor equipped with the channel field of the 1st conductivity-type semi-conductor formed in the path of the charge carrier between the source and both the fields of a drain, and the 2nd conductivity-type semiconductor region in which it is located in contact with the channel field, and said channel field equips with the undoping layer of the 1st conductivity type, and the 1st conductivity-type semi-conductor layer in which it is located in so that the undoping layer may face across a vertical side, and concentration distribution of the thickness direction projects in the shape of a pulse.
[Claim 2] The junction field effect transistor according to claim 1 in which said 2nd conductivity-type semiconductor region is either of the thin films formed a semi-conductor substrate and on the semi-conductor substrate, and said channel field is located in contact with the 2nd conductivity-type semiconductor region top.
[Claim 3] The junction field effect transistor according to claim 1 or 2 by which said 2nd conductivity-type semiconductor region introduces the 2nd conductivity-type impurity into either of the 1st conductivity-type semi-conductor film formed in contact with the 1st conductivity-type semi-conductor substrate and the semi-conductor substrate top by either ion-implantation and the impurity diffusion method, and is formed in it.
[Claim 4] The junction field effect transistor according to claim 1 or 2 which is the field in which said 2nd conductivity-type semiconductor region added and formed the 2nd conductivity-type impurity while carrying out epitaxial growth of the semi-conductor film in contact with said semi-conductor substrate top.
[Claim 5] A junction field effect transistor according to claim 1 to 3 with the thickness of said channel field thinner than the thickness of the depletion layer decided by diffusion potential of the joint of said channel field and said 2nd conductivity-type semiconductor region.
[Claim 6] The junction field effect transistor according to claim 1 to 5 said whose semi-conductor substrate is a SiC substrate and whose crystal which constitutes said each semi-conductor is SiC.
[Claim 7] It has a channel field for the path of the charge carrier between both the fields of the source and a drain. It is the manufacture approach of the junction field effect transistor which controls by gate voltage the flow of said charge carrier which passes through the channel field. To the n conductivity-type SiC thin film formed on said n conductivity-type SiC substrate or its n conductivity-type SiC substrate The process which introduces p conductivity-type impurity with ion-implantation, or carries out whether p conductivity-type impurity is added, and forms a p conductivity-type SiC layer into the epitaxial growth of a SiC thin film, It touches on said p conductivity-type SiC layer. The SiC undoping layer of n conductivity type, The manufacture

approach of a junction field effect transistor which is located so that the SiC undoping layer may face across the vertical side, and is equipped with the process which forms the channel layer containing the n conductivity-type SiC layer in which concentration distribution of the thickness direction projects in the shape of a pulse.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention more specifically relates to JFET which planned securing suppression and high conductance of the elevated-temperature leakage current, and its manufacture approach about a junction field effect transistor (JFET:Junction Field Effect Transistor) and its manufacture approach by considering the impurity atom concentration profile of a channel field as special distribution.
[0002]
[Description of the Prior Art] Conventionally, in JFET, as shown in drawing 8 , the source field 104 of n+ conductivity type linked to the source electrode S and the drain field 104 of n+ conductivity type linked to the drain electrode D are continuing in n conductivity-type field 103 where high impurity concentration is lower than it. The channel field 107 where especially the center section of the n conductivity-type field 103 was made thin in thickness at the pars basilaris ossis occipitalis of a slot 109 is formed. The above-mentioned configuration is prepared in contact with p+ conductivity-type layer 102 top formed on p+ conductivity-type semi-conductor substrate 101. Moreover, the gate electrode G is formed in the rear face of a semi-conductor substrate.
[0003] In using JFET of the above-mentioned configuration for a switching element, negative potential is impressed to the gate electrode G, and it impresses an electrical potential difference to the pn junction of p+ conductivity-type thin film 102 and the channel field 109. In order to realize an OFF state, let potential of n conductivity-type field be plus potential at the above-mentioned pn junction by making potential of a reverse bias electrical potential difference, i.e., p+ conductivity-type field, into minus potential. By adding impression of this reverse bias electrical potential difference to p+n junction, a depletion layer is grown up into n conductivity-type field 107,103, and the whole channel thickness is intercepted by the depletion layer. On the other hand, by making gate voltage into zero or a forward electrical potential difference, in order to realize an ON state, an electrical potential difference is impressed so that a charge carrier may move between source drains in a channel field.
[0004] In above-mentioned explanation, JFET explained by assuming that it is no MARION. That is, if no electrical potential differences are impressed to the source, a drain, and a gate electrode, a depletion layer did not ****** to a channel and the ON state is realized. However, the diffusion potential of the above-mentioned p+n junction is large, and when channel thickness is sufficiently thin, a depletion layer is formed of the reverse bias electrical potential difference resulting from diffusion potential covering the whole thickness of a channel field. In this case, an OFF state is realized even if it impresses an electrical potential difference to neither the source nor a drain nor a gate electrode. Such JFET that an OFF state realizes even if it does not impress

an electrical potential difference from the outside is called JFET of no MARIOFU.
[0005] Above JFET can be used as a high-speed switching element excellent in pressure resistance, if a SiC substrate is used as a semi-conductor substrate.
[0006]
[Problem(s) to be Solved by the Invention] However, the current which can be passed by the ON state cannot be decided by the thickness, width of face, and high impurity concentration (carrier concentration) of a channel field, and cannot pass usually so big a current. Moreover, if high impurity concentration of a channel field is made high in order to enlarge a current, the fall of component pressure-proofing may be brought about. When high impurity concentration of a channel field is made high, the overhang thickness of a depletion layer becomes small and it becomes impossible moreover, to realize no MARIOFU. On the contrary, if it is going to realize no MARIOFU, channel thickness must be made thin and high impurity concentration of a channel field must be made low. Consequently, it is not avoided that conductance becomes low.
[0007] On the other hand, in order to raise the electron mobility of semi-conductors, such as SiC, as shown in drawing 9 In undoping layer 107a of the channel field 107, concentration distribution of the thickness direction has discretely semi-conductor layer 107b of the shape of a delta function field. The so-called semi-conductor layer of a delta dope MESFET which it has () [Metal Semiconductor] Field Effect Transistor is proposed (Yokogawa et al.: collection of 48th applied-physics relation union lecture meeting lecture drafts 30 a-E -13 and J.of Applied Physics, Vol89, p.1794.). The identifier of a delta dope originates in the delta function showing distribution of the shape of a pulse, and the letter of a spike. Therefore, the above-mentioned concentration distribution may be called a delta dope or pulse dope. The channel field 107 containing the above-mentioned pulse-like high concentration semi-conductor layer is formed on the undoping SiC layer 102 formed on the SiC substrate 101.
[0008] In Above MESFET, although ohmic contact of the source electrode S and the drain electrode D is carried out to the n+SiC layer 104, the Schottky barrier of the gate electrode G and the undoping SiC layer 107b is carried out. The depletion-layer thickness of the Schottky barrier changes and the current which flows between the source and a drain field changes with the signals impressed to the gate electrode G. By having the channel field of such a delta dope, Above MESFET can have high electron mobility.
[0009] However, in MESFET which controls a current by the shot key electrode, since the obstruction potential of the Schottky barrier is low, if a temperature rise occurs, the leakage of a current will be produced. Moreover, as mentioned above, in a no MARIOFU mold, a depletion layer is jutted out with the diffusion potential which occurs spontaneously in the joint of a shot key electrode and a semi-conductor, a channel is intercepted, and it considers as an OFF state. Since the diffusion potential of the Schottky barrier is as low as about 1V, the overhang thickness of a depletion layer is small. For this reason, in order to make a channel intercept by this depletion layer, it is necessary to make channel thickness fairly thin. Consequently, channel on resistance will be large and conductance will become small.
[0010] This invention aims at realizing no MARIOFU easily and offering little JFET and its manufacture approach of the leakage current also at an elevated temperature, securing high conductance.
[0011]
[Means for Solving the Problem] JFET of this invention is JFET equipped with the channel field of the 1st conductivity-type semi-conductor formed in the path of the charge carrier between the source and both the fields of a drain, and the 2nd conductivity-type semiconductor region in

which it is located in contact with the channel field. A channel field is equipped with the undoping layer of the 1st conductivity type, and the 1st conductivity-type semi-conductor layer in which it is located in so that that undoping layer may face across a vertical side, and concentration distribution of the thickness direction projects in the shape of a pulse in this JFET (claim 1).

[0012] (The 2nd conductivity-type channel field / 1st conductivity-type semi-conductor layer) The diffusion potential of an interface is several times as large as the obstruction potential difference of the Schottky barrier. For example, when SiC is used for a semi-conductor, the Schottky barrier electrical potential differences with Ti are 1.1V-1.2V. As compared with this, the diffusion potential of pn junction reaches about 3 V. For this reason, the leakage current in an elevated temperature can be made lower in each stage than MESFET using the Schottky barrier.

[0013] Moreover, by formation of the 1st conductivity-type semi-conductor layer of thickness direction pulse-like high concentration distribution, electric resistance can be reduced and more currents can be passed. That is, high conductance is securable. furthermore, the slot which divides the source and a drain field since the maximum upper layer of a channel field is the 1st conductivity-type undoping layer -- RIE (Reactive Ion Etching) -- even if there is a dimension error, it can avoid almost influencing on resistance, when etching by law That is, when parallel connection of a high resistive layer and the low resistive layer is carried out, even if a high resistive layer has some fluctuation, effect hardly receives combined resistance. For this reason, the tolerance of the process tolerance of RIE can be raised and the manufacture yield can be raised. Moreover, since electron mobility is also dependent on the concentration of an undoping layer, high electron mobility is securable. In addition, as long as it is contacted so that the above-mentioned undoping layer may face across the vertical side, there may be one or more-layer how many layers of 1st conductivity-type semi-conductor layers which have the concentration distribution projected in the shape of a pulse in the above-mentioned thickness direction. Moreover, it is made for the thickness of a high-concentration layer to have several [several / 1// of an undoping layer], for example, the thickness of 1/5, in the shape of an above-mentioned pulse.

[0014] In JFET of above-mentioned this invention, the 2nd conductivity-type semiconductor region is either of the thin films formed a semi-conductor substrate and on the semi-conductor substrate, and a channel field can be located in contact with the 2nd conductivity-type semiconductor region top (claim 2).

[0015] A depletion layer can be jutted out of the inferior surface of tongue of a channel field, and the flow of a charge carrier can be easily controlled by this configuration. The gate electrode over which impress a reverse bias electrical potential difference to the above-mentioned joint, and a depletion layer is made to jut out can have the next arrangement. (a) It is good also as backgate structure of connecting a gate electrode to the rear face of a channel and the semi-conductor substrate of the opposite side, and good also as structure of connecting a gate electrode to both both [one side or] of both the sides of the same side as the (b) channel.

[0016] In JFET of above-mentioned this invention, it can do with what introduced the 2nd conductivity-type impurity into either of the 1st conductivity-type semi-conductor film formed in the 2nd conductivity-type semiconductor region in contact with the 1st conductivity-type semi-conductor substrate and the semi-conductor substrate top by either ion-implantation and the impurity diffusion method, and was formed in it (claim 3).

[0017] When the p conductivity-type SiC film forms boron with an epitaxial grown method as a dopant, only a very bad thing may be able to do crystallinity, including a micro pipe etc. mostly.

Moreover, since aluminum deposits on the wall of membrane formation equipment when making aluminum into a dopant, it is necessary to clean periodically and manufacture efficiency falls. Even when a semi-conductor is set to SiC and the 2nd conductivity type is used as p conductivity type by the above-mentioned manufacture approach, a crystalline good p conductivity-type SiC layer can be formed in the bottom of a channel field under infallible high productivity. Consequently, the leakage current in an elevated temperature can be controlled.

[0018] In JFET of above-mentioned this invention, while carrying out epitaxial growth of the semi-conductor film for the 2nd conductivity-type semiconductor region in contact with a semi-conductor substrate top, it can consider as the field which added and formed the 2nd conductivity-type impurity (claim 4).

[0019] By this configuration, when the conditions to which epitaxial growth for example, of the p conductivity-type SiC film is carried out without a serious defect are able to be found out, this p conductivity-type SiC film can be used, and JFET can be formed.

[0020] In JFET of above-mentioned this invention, the thickness of a channel field can make it thinner than the thickness of the depletion layer decided by diffusion potential of the joint of a channel field and the 2nd conductivity-type semiconductor region (claim 5).

[0021] By this configuration, the 1st conductivity-type high impurity concentration of (1) undoping layer, the 1st conductivity-type high impurity concentration of (2) delta dope layer, and the 2nd conductivity-type high impurity concentration of the (3) 2nd conductivity-type semi-conductor layer can be adjusted, the diffusion potential of a joint can be known, and the thickness of the depletion layer jutted out over a channel side in a joint can be known. JFET of no MARIOFU can be manufactured by making thickness of (4) channel field thinner than the thickness of this depletion layer. Since JFET of no MARIOFU is made with an OFF state when failure is produced in an electrical circuit system and electricity is not supplied, it can be used for control of a rotating machine etc., without complicating a circuit.

[0022] In JFET of above-mentioned this invention, a semi-conductor substrate is used as a SiC substrate, and the crystal which constitutes each semi-conductor is made with SiC (claim 6).

[0023] SiC is excellent in the proof-pressure engine performance, and since the mobility of a charge carrier is also high, it can use for the high-speed switching element of control of large power, or large power.

[0024] It is the manufacture approach of the junction field effect transistor which controls the flow of the charge carrier which has a channel field for the path of the charge carrier between both the fields of the source and a drain, and passes through the channel field with gate voltage by the manufacture approach of JFET of this invention. This manufacture approach to the n conductivity-type SiC thin film formed on an n conductivity-type SiC substrate or its n conductivity-type SiC substrate The process which introduces p conductivity-type impurity by either ion-implantation and the diffusion method, or carries out whether p conductivity-type impurity is added, and forms a p conductivity-type SiC layer into the epitaxial growth of a SiC thin film, In contact with a p conductivity-type SiC layer top, it has the process which forms the channel layer containing the SiC undoping layer of n conductivity type, and the n conductivity-type SiC layer in which it is located in so that the SiC undoping layer may face across the vertical side, and concentration distribution of the thickness direction projects in the shape of a pulse (claim 7).

[0025] JFET which secured high conductance can be easily formed by formation of the 1st conductivity-type semi-conductor layer of high concentration distribution of the shape of a thickness direction pulse which was excellent in crystallinity by this manufacture approach.

furthermore, the case where the slot which divides the source and a drain field, for example is formed since the maximum upper layer of a channel field is the 1st conductivity-type undoping layer -- RIE (Reactive Ion Etching) -- even if there is a dimension error, it can avoid almost influencing on resistance, when etching by law That is, when parallel connection of a high resistive layer and the low resistive layer is carried out, even if a high resistive layer has some fluctuation, effect hardly receives combined resistance. For this reason, the tolerance of the process tolerance of RIE can be raised and the manufacture yield can be raised.
[0026]
[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained using a drawing.
(Gestalt 1 of operation) Drawing 1 is the sectional view showing JFET in the gestalt 1 of operation of this invention. The p+ conductivity-type SiC film 2 is formed on the SiC substrate 1. On the p+ conductivity-type SiC film 2, the laminating of n with a thickness of 50nm which is undoping layer conductivity-type SiC film 5a, and the pulse-like layer 5b of n+ conductivity type which has steep concentration distribution with a thickness of 10nm is carried out by turns. Distribution of n conductivity-type high impurity concentration of the thickness direction of a channel field is shown in drawing 2 . This laminating field constitutes the channel field 5. Pulse-like layer 5b of n+ conductivity type may call it a delta layer, a pulse-like layer, or the letter layer of a spike. The peak value of n mold high impurity concentration of this delta layer is 1x1018cm-3. n conductivity-type high impurity concentration of an undoping layer -- the concentration of this peak value -- number order -- it is low. The part of the bottom which touches the part of the top of the channel layer 5 and the p+ conductivity-type SiC film 2 is formed of the undoping layer.
[0027] n+ conductivity-type field 4 linked to the source electrode S divided and located on the channel layer 5 and the drain electrode D and n conductivity-type semiconductor region 3 which is located in the bottom of it and touches a channel field are arranged.
[0028] In the case of the structure of drawing 1 , the gate electrode G is arranged on the p+ conductivity-type SiC film formed on the SiC substrate.
[0029] In JFET of the above-mentioned structure, the diffusion potential of about 3 V is produced in the joint of the p+ conductivity-type SiC film 2 and undoping layer 5a of the lowest layer of a channel field. Since this diffusion potential acts on the above-mentioned joint as a reverse bias electrical potential difference, it can control the leakage current certainly to an elevated temperature more compared with the leakage current prevention by the Schottky barrier potential of MESFET. Furthermore, by formation of the delta layer of a high concentration impurity, electric resistance can be reduced and more currents can be passed. That is, high conductance is securable. Moreover, since it depends also for electronic mobility on the concentration of an undoping layer, high electron mobility is securable.
[0030] The structure of above-mentioned drawing 1 can be manufactured by the following manufacture approach.
(1) Do introduce p conductivity-type impurity into the n conductivity-type SiC film formed on the n conductivity-type SiC substrate or the SiC substrate with ion-implantation first? Or the SiC film is grown epitaxially adding p conductivity-type impurity, and a p conductivity-type SiC layer is formed. Consequently, the crystalline good p conductivity-type SiC film can be obtained.
(2) Subsequently, form an n conductivity-type undoping SiC layer and a pulse-like n conductivity-type SiC layer by turns. The lowest layer and the maximum upper layer of a channel field are taken as an undoping layer. Peak value of pulse-like n conductivity-type high

impurity concentration is set to 1x1018cm-3.
(3) Form the n conductivity-type SiC layer used as the source and a drain field after this. Patterning of the channel field 5 is carried out by etching this n conductivity-type SiC film by dry etching, such as RIE (Reactive Ion Etching).
(4) Subsequently, separate and form the source and a drain on a channel field by the usual approach. Moreover, the gate electrode G is formed on the p+ conductivity-type SiC film 2.
[0031] By the above-mentioned manufacture approach, the good crystalline p conductivity-type SiC film can be obtained.
[0032] Drawing 3 is drawing showing the modification of JFET of the gestalt 1 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity was introduced into the SiC substrate, and the channel field 5 is directly arranged on it.
[0033] Moreover, drawing 4 is drawing showing another modification of JFET of the gestalt 1 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity is introduced into a SiC substrate, and it considers as a p conductivity-type SiC substrate. Furthermore, the gate electrode is made into the backgate structure by which ohmic contact was carried out to the rear-face side of an n+ conductivity-type SiC substrate. By using such backgate structure, the two-dimensional dimension of JFET is reduced and it becomes possible to miniaturize.
(Gestalt 2 of operation) Drawing 5 is the sectional view showing JFET in the gestalt 2 of operation of this invention. This JFET is JFET of a no MARIOFU mold, and, for this reason, the layer of pulse-like concentration is made only into one layer. Let thickness of the channel field 5 which consists of pulse-like high concentration n-type-semiconductor one-layer layer 5b and n conductivity-type undoping layer 5a which sandwiches it from the upper and lower sides be the thickness by which no MARIOFU is realized. That is, for the diffusion potential generated in the joint of a channel field and a p+ conductivity-type SiC layer, a depletion layer occurs in this joint and only predetermined thickness is extended to a channel field. If the above-mentioned channel field is intercepted by the depletion layer of this predetermined thickness, JFET of no MARIOFU will be realized by it.
[0034] In SiC, the above-mentioned diffusion potential is comparatively as high as about 3 V. Since the shot key potentials in MESFET are 1.1V-1.2V, several times as high a reverse bias electrical potential difference as it can be obtained. Since the thickness of the above-mentioned depletion layer is proportional to a reverse bias electrical potential difference, since diffusion potential abbreviation 3V of JFET are fairly higher from the shot key electrical potential difference 1.1 of MESFET, it can make channel thickness thicker than before, and it can form JFET. For this reason, the way of JFET of no MARIOFU can secure high conductance from MESFET of no MARIOFU.
[0035] Drawing 6 [JFET of no MARIOFU of drawing 5] which can be fundamentally manufactured by the same manufacture approach as JFET of drawing 1 is drawing showing the modification of JFET of no MARIOFU in the gestalt 2 of operation of above-mentioned this invention. In this JFET, the p conductivity-type SiC substrate which introduced p conductivity-type impurity into the SiC substrate is used. For this reason, since it is not necessary to form the p+ conductivity-type SiC film on a SiC substrate, 1 process abbreviation can be carried out.
[0036] Moreover, drawing 7 is drawing showing another modification of JFET of no MARIOFU in the gestalt 2 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity is introduced into a SiC substrate, and the p conductivity-type SiC substrate is used. Furthermore, the gate electrode is made into the backgate structure by which ohmic contact was

carried out to the rear-face side of an n+ conductivity-type SiC substrate. By using such backgate structure, the two-dimensional dimension of JFET is reduced and it becomes possible to miniaturize.

[0037] In the above, although the gestalt of operation of this invention was explained, the gestalt of operation of this invention indicated above is instantiation to the last, and the range of this invention is not limited to the gestalt of implementation of these invention. The range of this invention is shown by the publication of a claim, and includes all modification in the publication of a claim, equal semantics, and within the limits further.

[0038]

[Effect of the Invention] By using JFET and its manufacture approach of this invention, securing high conductance, no MARIOFU can be realized easily and JFET with little leakage current can be offered also at an elevated temperature.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention more specifically relates to JFET which planned securing suppression and high conductance of the elevated-temperature leakage current, and its manufacture approach about a junction field effect transistor (JFET:Junction Field Effect Transistor) and its manufacture approach by considering the impurity atom concentration profile of a channel field as special distribution.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, in JFET, as shown in drawing 8 , the source field 104 of n+ conductivity type linked to the source electrode S and the drain field 104 of n+ conductivity type linked to the drain electrode D are continuing in n conductivity-type field 103 where high impurity concentration is lower than it. The channel field 107 where especially the center section of the n conductivity-type field 103 was made thin in thickness at the pars basilaris ossis occipitalis of a slot 109 is formed. The above-mentioned configuration is prepared in contact with p+ conductivity-type layer 102 top formed on p+ conductivity-type semi-conductor substrate 101. Moreover, the gate electrode G is formed in the rear face of a semi-conductor substrate.

[0003] In using JFET of the above-mentioned configuration for a switching element, negative potential is impressed to the gate electrode G, and it impresses an electrical potential difference to the pn junction of p+ conductivity-type thin film 102 and the channel field 109. In order to realize an OFF state, let potential of n conductivity-type field be plus potential at the above-mentioned pn junction by making potential of a reverse bias electrical potential difference, i.e., p+ conductivity-type field, into minus potential. By adding impression of this reverse bias electrical potential difference to p+n junction, a depletion layer is grown up into n conductivity-type field 107,103, and the whole channel thickness is intercepted by the depletion layer. On the other hand, by making gate voltage into zero or a forward electrical potential difference, in order to realize an ON state, an electrical potential difference is impressed so that a charge carrier may move between source drains in a channel field.

[0004] In above-mentioned explanation, JFET explained by assuming that it is no MARION. That is, if no electrical potential differences are impressed to the source, a drain, and a gate electrode, a depletion layer did not ****** to a channel and the ON state is realized. However, the diffusion potential of the above-mentioned p+n junction is large, and when channel thickness is sufficiently thin, a depletion layer is formed of the reverse bias electrical potential difference resulting from diffusion potential covering the whole thickness of a channel field. In this case, an OFF state is realized even if it impresses an electrical potential difference to neither the source nor a drain nor a gate electrode. Such JFET that an OFF state realizes even if it does not impress an electrical potential difference from the outside is called JFET of no MARIOFU.

[0005] Above JFET can be used as a high-speed switching element excellent in pressure resistance, if a SiC substrate is used as a semi-conductor substrate.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] By using JFET and its manufacture approach of this invention, securing high conductance, no MARIOFU can be realized easily and JFET with little leakage current can be offered also at an elevated temperature.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the current which can be passed by the ON state cannot be decided by the thickness, width of face, and high impurity concentration (carrier concentration) of a channel field, and cannot pass usually so big a current. Moreover, if high impurity concentration of a channel field is made high in order to enlarge a current, the fall of component pressure-proofing may be brought about. When high impurity concentration of a channel field is made high, the overhang thickness of a depletion layer becomes small and it becomes impossible moreover, to realize no MARIOFU. On the contrary, if it is going to realize no MARIOFU, channel thickness must be made thin and high impurity concentration of a channel field must be made low. Consequently, it is not avoided that conductance becomes low.
[0007] On the other hand, in order to raise the electron mobility of semi-conductors, such as SiC, as shown in drawing 9 In undoping layer 107a of the channel field 107, concentration distribution of the thickness direction has discretely semi-conductor layer 107b of the shape of a delta function field. The so-called semi-conductor layer of a delta dope MESFET which it has () [Metal Semiconductor] Field Effect Transistor is proposed (Yokogawa et al.: collection of 48th applied-physics relation union lecture meeting lecture drafts 30 a-E -13 and J.of Applied Physics, Vol89, p.1794.). The identifier of a delta dope originates in the delta function showing distribution of the shape of a pulse, and the letter of a spike. Therefore, the above-mentioned concentration distribution may be called a delta dope or pulse dope. The channel field 107 containing the above-mentioned pulse-like high concentration semi-conductor layer is formed on the undoping SiC layer 102 formed on the SiC substrate 101.
[0008] In Above MESFET, although ohmic contact of the source electrode S and the drain electrode D is carried out to the n+SiC layer 104, the Schottky barrier of the gate electrode G and the undoping SiC layer 107b is carried out. The depletion-layer thickness of the Schottky barrier changes and the current which flows between the source and a drain field changes with the signals impressed to the gate electrode G. By having the channel field of such a delta dope, Above MESFET can have high electron mobility.
[0009] However, in MESFET which controls a current by the shot key electrode, since the obstruction potential of the Schottky barrier is low, if a temperature rise occurs, the leakage of a current will be produced. Moreover, as mentioned above, in a no MARIOFU mold, a depletion layer is jutted out with the diffusion potential which occurs spontaneously in the joint of a shot key electrode and a semi-conductor, a channel is intercepted, and it considers as an OFF state. Since the diffusion potential of the Schottky barrier is as low as about 1V, the overhang thickness of a depletion layer is small. For this reason, in order to make a channel intercept by this depletion layer, it is necessary to make channel thickness fairly thin. Consequently, channel on resistance will be large and conductance will become small.
[0010] This invention aims at realizing no MARIOFU easily and offering little JFET and its

manufacture approach of the leakage current also at an elevated temperature, securing high conductance.
[0011]

[Translation done.]

MEANS

[Means for Solving the Problem] JFET of this invention is JFET equipped with the channel field of the 1st conductivity-type semi-conductor formed in the path of the charge carrier between the source and both the fields of a drain, and the 2nd conductivity-type semiconductor region in which it is located in contact with the channel field. A channel field is equipped with the undoping layer of the 1st conductivity type, and the 1st conductivity-type semi-conductor layer in which it is located in so that that undoping layer may face across a vertical side, and concentration distribution of the thickness direction projects in the shape of a pulse in this JFET (claim 1).
[0012] (The 2nd conductivity-type channel field / 1st conductivity-type semi-conductor layer) The diffusion potential of an interface is several times as large as the obstruction potential difference of the Schottky barrier. For example, when SiC is used for a semi-conductor, the Schottky barrier electrical potential differences with Ti are 1.1V-1.2V. As compared with this, the diffusion potential of pn junction reaches about 3 V. For this reason, the leakage current in an elevated temperature can be made lower in each stage than MESFET using the Schottky barrier.
[0013] Moreover, by formation of the 1st conductivity-type semi-conductor layer of thickness direction pulse-like high concentration distribution, electric resistance can be reduced and more currents can be passed. That is, high conductance is securable. furthermore, the slot which divides the source and a drain field since the maximum upper layer of a channel field is the 1st conductivity-type undoping layer -- RIE (Reactive Ion Etching) -- even if there is a dimension error, it can avoid almost influencing on resistance, when etching by law That is, when parallel connection of a high resistive layer and the low resistive layer is carried out, even if a high resistive layer has some fluctuation, effect hardly receives combined resistance. For this reason, the tolerance of the process tolerance of RIE can be raised and the manufacture yield can be raised. Moreover, since electron mobility is also dependent on the concentration of an undoping layer, high electron mobility is securable. In addition, as long as it is contacted so that the above-mentioned undoping layer may face across the vertical side, there may be one or more-layer how many layers of 1st conductivity-type semi-conductor layers which have the concentration distribution projected in the shape of a pulse in the above-mentioned thickness direction. Moreover, it is made for the thickness of a high-concentration layer to have several [several / 1// of an undoping layer], for example, the thickness of 1/5, in the shape of an above-mentioned pulse.
[0014] In JFET of above-mentioned this invention, the 2nd conductivity-type semiconductor region is either of the thin films formed a semi-conductor substrate and on the semi-conductor substrate, and a channel field can be located in contact with the 2nd conductivity-type semiconductor region top (claim 2).
[0015] A depletion layer can be jutted out of the inferior surface of tongue of a channel field, and

the flow of a charge carrier can be easily controlled by this configuration. The gate electrode over which impress a reverse bias electrical potential difference to the above-mentioned joint, and a depletion layer is made to jut out can have the next arrangement. (a) It is good also as backgate structure of connecting a gate electrode to the rear face of a channel and the semi-conductor substrate of the opposite side, and good also as structure of connecting a gate electrode to both both [one side or] of both the sides of the same side as the (b) channel.

[0016] In JFET of above-mentioned this invention, it can do with what introduced the 2nd conductivity-type impurity into either of the 1st conductivity-type semi-conductor film formed in the 2nd conductivity-type semiconductor region in contact with the 1st conductivity-type semi-conductor substrate and the semi-conductor substrate top by either ion-implantation and the impurity diffusion method, and was formed in it (claim 3).

[0017] When the p conductivity-type SiC film forms boron with an epitaxial grown method as a dopant, only a very bad thing may be able to do crystallinity, including a micro pipe etc. mostly. Moreover, since aluminum deposits on the wall of membrane formation equipment when making aluminum into a dopant, it is necessary to clean periodically and manufacture efficiency falls. Even when a semi-conductor is set to SiC and the 2nd conductivity type is used as p conductivity type by the above-mentioned manufacture approach, a crystalline good p conductivity-type SiC layer can be formed in the bottom of a channel field under infallible high productivity. Consequently, the leakage current in an elevated temperature can be controlled.

[0018] In JFET of above-mentioned this invention, while carrying out epitaxial growth of the semi-conductor film for the 2nd conductivity-type semiconductor region in contact with a semi-conductor substrate top, it can consider as the field which added and formed the 2nd conductivity-type impurity (claim 4).

[0019] By this configuration, when the conditions to which epitaxial growth for example, of the p conductivity-type SiC film is carried out without a serious defect are able to be found out, this p conductivity-type SiC film can be used, and JFET can be formed.

[0020] In JFET of above-mentioned this invention, the thickness of a channel field can make it thinner than the thickness of the depletion layer decided by diffusion potential of the joint of a channel field and the 2nd conductivity-type semiconductor region (claim 5).

[0021] By this configuration, the 1st conductivity-type high impurity concentration of (1) undoping layer, the 1st conductivity-type high impurity concentration of (2) delta dope layer, and the 2nd conductivity-type high impurity concentration of the (3) 2nd conductivity-type semi-conductor layer can be adjusted, the diffusion potential of a joint can be known, and the thickness of the depletion layer jutted out over a channel side in a joint can be known. JFET of no MARIOFU can be manufactured by making thickness of (4) channel field thinner than the thickness of this depletion layer. Since JFET of no MARIOFU is made with an OFF state when failure is produced in an electrical circuit system and electricity is not supplied, it can be used for control of a rotating machine etc., without complicating a circuit.

[0022] In JFET of above-mentioned this invention, a semi-conductor substrate is used as a SiC substrate, and the crystal which constitutes each semi-conductor is made with SiC (claim 6).

[0023] SiC is excellent in the proof-pressure engine performance, and since the mobility of a charge carrier is also high, it can use for the high-speed switching element of control of large power, or large power.

[0024] It is the manufacture approach of the junction field effect transistor which controls the flow of the charge carrier which has a channel field for the path of the charge carrier between both the fields of the source and a drain, and passes through the channel field with gate voltage

by the manufacture approach of JFET of this invention. This manufacture approach to the n conductivity-type SiC thin film formed on an n conductivity-type SiC substrate or its n conductivity-type SiC substrate The process which introduces p conductivity-type impurity by either ion-implantation and the diffusion method, or carries out whether p conductivity-type impurity is added, and forms a p conductivity-type SiC layer into the epitaxial growth of a SiC thin film, In contact with a p conductivity-type SiC layer top, it has the process which forms the channel layer containing the SiC undoping layer of n conductivity type, and the n conductivity-type SiC layer in which it is located in so that the SiC undoping layer may face across the vertical side, and concentration distribution of the thickness direction projects in the shape of a pulse (claim 7).

[0025] JFET which secured high conductance can be easily formed by formation of the 1st conductivity-type semi-conductor layer of high concentration distribution of the shape of a thickness direction pulse which was excellent in crystallinity by this manufacture approach. furthermore, the case where the slot which divides the source and a drain field, for example is formed since the maximum upper layer of a channel field is the 1st conductivity-type undoping layer -- RIE (Reactive Ion Etching) -- even if there is a dimension error, it can avoid almost influencing on resistance, when etching by law That is, when parallel connection of a high resistive layer and the low resistive layer is carried out, even if a high resistive layer has some fluctuation, effect hardly receives combined resistance. For this reason, the tolerance of the process tolerance of RIE can be raised and the manufacture yield can be raised.

[0026]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained using a drawing.

(Gestalt 1 of operation) Drawing 1 is the sectional view showing JFET in the gestalt 1 of operation of this invention. The p+ conductivity-type SiC film 2 is formed on the SiC substrate 1. On the p+ conductivity-type SiC film 2, the laminating of n with a thickness of 50nm which is undoping layer conductivity-type SiC film 5a, and the pulse-like layer 5b of n+ conductivity type which has steep concentration distribution with a thickness of 10nm is carried out by turns. Distribution of n conductivity-type high impurity concentration of the thickness direction of a channel field is shown in drawing 2 . This laminating field constitutes the channel field 5. Pulse-like layer 5b of n+ conductivity type may call it a delta layer, a pulse-like layer, or the letter layer of a spike. The peak value of n mold high impurity concentration of this delta layer is 1x1018cm-3. n conductivity-type high impurity concentration of an undoping layer -- the concentration of this peak value -- number order -- it is low. The part of the bottom which touches the part of the top of the channel layer 5 and the p+ conductivity-type SiC film 2 is formed of the undoping layer.

[0027] n+ conductivity-type field 4 linked to the source electrode S divided and located on the channel layer 5 and the drain electrode D and n conductivity-type semiconductor region 3 which is located in the bottom of it and touches a channel field are arranged.

[0028] In the case of the structure of drawing 1 , the gate electrode G is arranged on the p+ conductivity-type SiC film formed on the SiC substrate.

[0029] In JFET of the above-mentioned structure, the diffusion potential of about 3 V is produced in the joint of the p+ conductivity-type SiC film 2 and undoping layer 5a of the lowest layer of a channel field. Since this diffusion potential acts on the above-mentioned joint as a reverse bias electrical potential difference, it can control the leakage current certainly to an elevated temperature more compared with the leakage current prevention by the Schottky barrier

potential of MESFET. Furthermore, by formation of the delta layer of a high concentration impurity, electric resistance can be reduced and more currents can be passed. That is, high conductance is securable. Moreover, since it depends also for electronic mobility on the concentration of an undoping layer, high electron mobility is securable.
[0030] The structure of above-mentioned drawing 1 can be manufactured by the following manufacture approach.
(1) Do introduce p conductivity-type impurity into the n conductivity-type SiC film formed on the n conductivity-type SiC substrate or the SiC substrate with ion-implantation first? Or the SiC film is grown epitaxially adding p conductivity-type impurity, and a p conductivity-type SiC layer is formed. Consequently, the crystalline good p conductivity-type SiC film can be obtained.
(2) Subsequently, form an n conductivity-type undoping SiC layer and a pulse-like n conductivity-type SiC layer by turns. The lowest layer and the maximum upper layer of a channel field are taken as an undoping layer. Peak value of pulse-like n conductivity-type high impurity concentration is set to 1x1018cm-3.
(3) Form the n conductivity-type SiC layer used as the source and a drain field after this. Patterning of the channel field 5 is carried out by etching this n conductivity-type SiC film by dry etching, such as RIE (Reactive Ion Etching).
(4) Subsequently, separate and form the source and a drain on a channel field by the usual approach. Moreover, the gate electrode G is formed on the p+ conductivity-type SiC film 2.
[0031] By the above-mentioned manufacture approach, the good crystalline p conductivity-type SiC film can be obtained.
[0032] Drawing 3 is drawing showing the modification of JFET of the gestalt 1 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity was introduced into the SiC substrate, and the channel field 5 is directly arranged on it.
[0033] Moreover, drawing 4 is drawing showing another modification of JFET of the gestalt 1 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity is introduced into a SiC substrate, and it considers as a p conductivity-type SiC substrate. Furthermore, the gate electrode is made into the backgate structure by which ohmic contact was carried out to the rear-face side of an n+ conductivity-type SiC substrate. By using such backgate structure, the two-dimensional dimension of JFET is reduced and it becomes possible to miniaturize.
(Gestalt 2 of operation) Drawing 5 is the sectional view showing JFET in the gestalt 2 of operation of this invention. This JFET is JFET of a no MARIOFU mold, and, for this reason, the layer of pulse-like concentration is made only into one layer. Let thickness of the channel field 5 which consists of pulse-like high concentration n-type-semiconductor one-layer layer 5b and n conductivity-type undoping layer 5a which sandwiches it from the upper and lower sides be the thickness by which no MARIOFU is realized. That is, for the diffusion potential generated in the joint of a channel field and a p+ conductivity-type SiC layer, a depletion layer occurs in this joint and only predetermined thickness is extended to a channel field. If the above-mentioned channel field is intercepted by the depletion layer of this predetermined thickness, JFET of no MARIOFU will be realized by it.
[0034] In SiC, the above-mentioned diffusion potential is comparatively as high as about 3 V. Since the shot key potentials in MESFET are 1.1V-1.2V, several times as high a reverse bias electrical potential difference as it can be obtained. Since the thickness of the above-mentioned depletion layer is proportional to a reverse bias electrical potential difference, since diffusion potential abbreviation 3V of JFET are fairly higher from the shot key electrical potential

difference 1.1 of MESFET, it can make channel thickness thicker than before, and it can form JFET. For this reason, the way of JFET of no MARIOFU can secure high conductance from MESFET of no MARIOFU.

[0035] Drawing 6 [JFET of no MARIOFU of drawing 5] which can be fundamentally manufactured by the same manufacture approach as JFET of drawing 1 is drawing showing the modification of JFET of no MARIOFU in the gestalt 2 of operation of above-mentioned this invention. In this JFET, the p conductivity-type SiC substrate which introduced p conductivity-type impurity into the SiC substrate is used. For this reason, since it is not necessary to form the p+ conductivity-type SiC film on a SiC substrate, 1 process abbreviation can be carried out.

[0036] Moreover, drawing 7 is drawing showing another modification of JFET of no MARIOFU in the gestalt 2 of operation of above-mentioned this invention. In this JFET, p conductivity-type impurity is introduced into a SiC substrate, and the p conductivity-type SiC substrate is used. Furthermore, the gate electrode is made into the backgate structure by which ohmic contact was carried out to the rear-face side of an n+ conductivity-type SiC substrate. By using such backgate structure, the two-dimensional dimension of JFET is reduced and it becomes possible to miniaturize.

[0037] In the above, although the gestalt of operation of this invention was explained, the gestalt of operation of this invention indicated above is instantiation to the last, and the range of this invention is not limited to the gestalt of implementation of these invention. The range of this invention is shown by the publication of a claim, and includes all modification in the publication of a claim, equal semantics, and within the limits further.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of JFET in the gestalt 1 of operation of this invention.

[Drawing 2] It is drawing showing distribution of n conductivity-type high impurity concentration of the thickness direction of a channel field.

[Drawing 3] It is the sectional view of the modification of JFET in the gestalt 1 of operation of this invention.

[Drawing 4] It is the sectional view of still more nearly another modification of JFET in the gestalt 1 of operation of this invention.

[Drawing 5] It is the sectional view of JFET in the gestalt 2 of operation of this invention.

[Drawing 6] It is the sectional view of the modification of JFET in the gestalt 2 of operation of this invention.

[Drawing 7] It is the sectional view of still more nearly another modification of JFET in the gestalt 2 of operation of this invention.

[Drawing 8] It is the sectional view showing the conventional JFET.

[Drawing 9] It is the sectional view showing the conventional MESFET.

[Description of Notations]

1 A SiC substrate, 2 The p+ conductivity-type SiC film, 3 An n conductivity-type SiC layer, 4 An n conductivity-type SiC layer, 5 A channel layer, 5a n conductivity-type undoping layer, 5b A pulse-like high concentration n mold SiC layer, S A source electrode, D A drain electrode, G Gate electrode.

[Translation done.]

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(54) ELECTRIC FIELD EFFECT TRANSISTOR

(57)Abstract:
PURPOSE: To produce a FET superior in high-frequency characteristic by providing an intrinsic or high-resistance semiconductor layer between a N-type channel and a P-type gate and depleting all channel layers in case of zero voltage across the gate and the source.
CONSTITUTION: Intrinsic or high-resistance N- epi-layer 21 is provided on P++ layer 20, and ions are implanted by using an oxide mask having thin film part 22a to form selectively P+ layer 23. Separately, an aperture is provided in film 22 to diffuse N+ layer 24. After that, large aperture 22c is provided to diffuse selectively N+ layer 24, and one side of diffusion is linked with layer 24. Next, mask 22 is removed, and layer 26 similar to layer 21 is formed epitaxially and is covered with oxide film 27. Apertures are selectively provided in film 27 to provide N+ layers 28 and 29 and P+ layer 30 which reach the edge of layers 24 and 25, and electrode SDG is formed respectively. By this constitution, the figure of merit of a Schottky barrier gate-type FET is enhanced to make the high-frequency characteristic good

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